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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,605	LEONG ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-19 and 28-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-19 and 28-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02-28-05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 8, 9, 12-14, 16, 18, 19 and 31-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marlin (US Pat. 6429046) in view of Paunovic et al. (US Pat. 5294486) and admitted prior art (APA).

A. Regarding claims 1-5, 8, 9, 12 and 13, Marlin et al. disclose a flip chip bumped device having a plurality of solder bumps/balls on respective under bump metal (UBM) pad structure (Fig. 1-6; Col. 1, lines 20-25; Col. 1, line 55- Col. 3, line 18) comprising:

- a flip chip substrate/FCS (see 102 in Fig. 5 and 6) including a first major/top surface and a second/bottom major surface
- the UBM pad structure including pads/array of pads being made of an electrically conductive/metal material (302/304/308 in Fig. 5 and 6) on a copper pad (see 104 in Fig. 5 and 6; Col. 1, line 60) and being positioned on the first/top surface,

the UBM pad structure (302/304/308 in Fig. 5 and 6) comprising a plurality of layers including:

- a solderable oxidation/diffusion retarding layer (304 in Fig. 5; Col. 2, lines 33-36) made of a material such as nickel to retard the rate of oxidation/diffusion of species/electrically conductive material from the pad structure
- an adhesion/binding/non-wettable layer (302 in Fig. 5 and 6) for binding the oxidation retarding layer to the conductive material of the pad, the adhesion/binding/non-wettable layer including titanium (Ti) or titanium-tungsten (Col. 2, lines 5-15), and
- a solder support/receiving layer (308 in Fig. 5 and 6) such as gold (Col. 2, line 61) being placed on the oxidation/diffusion retarding layer

- the above UBM structure providing the layers/means to prevent diffusion of material into the copper pad and the chip, dissolving of the copper and that for adhering/binding the pad, and
- a solder bump/ball (310 in Fig. 5 and 6) being attached/formed on the copper pad, the solder including a tin (Sn) based lead-free solder (Col. 2, line 19)

(Fig. 5/6; Fig. 1-6; Col. 1-3).

Marlin fails to:

- a) explicitly teach the device having the pads having the solder ball being in a form of a ball grid array (BGA), and
- b) teach the diffusion retarding layer being functional as the layer for controlling out-diffusion of the electrically conductive material from the at least one pad to the solder ball.

a) APA teaches conventional flip chip device being in a conventional BGA configuration (see specification pages 1 and 2).

b) Paunovic et al. disclose a prior art (see Col. 1, lines 50-65 in Paunovic et al.; the prior art: US Pat. 4016050, Lesh et al.) disclosing a conventional diffusion barrier structure wherein a diffusion retarding layer such as nickel having a predetermine thickness is used to control/retard diffusion/out-diffusion of copper from an underlying conductor/pad layer and to provide improved soldering/bonding (see the prior art: Lesh et al, Col. 3, lines 23-37, Abstract and Col. 5, line 20- Col. 6, line 16).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the elements a) and b) as taught by the APA and Paunovic et al. so that the improved diffusion barrier, solderability and interconnect reliability can be achieved in the APA and Marlin's device.

B. Regarding claim 1, using the diffusion retarding layer to prevent the out-diffusion during the solder reflow process do not distinguish over Marlin, Paunovic et al. and APA, because only the final product/structure is relevant, not preventing the out-diffusion during "solder reflow process", "solder pre-heat ramp-up process" or "environmetal/thermal cycling process". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claims 14, 16, 18, 19 and 31-40, Marlin, Paunovic et al. and APA teach substantially the entire claimed structure as applied to claim 1 above.

3. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marlin (US Pat. 6429046), Paunovic et al. (US Pat. 5294486) and APA as applied to claim 1 above, and further in view of Andricacos et al. (US Pat. 6224690).

Regarding claims 10 and 11, Marlin, Paunovic et al. and APA teach substantially the entire claimed structure as applied to claim 1 above, except the binding layer having a thickness in a range of 80- 120 nm or 90-110 nm respectively.

Andricacos et al. teach a flip chip/BGA device having an UBM structure, the UBM structure including conventional adhesion/binding layers comprising titanium, chromium, etc., the adhesion/binding layer having a thickness of about 100 nm to provide the desired adhesion and barrier properties (Col. 4, lines 45-55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the binding layer having a thickness in a range of 80-120 nm or 90-110 nm as taught by Andricacos et al. so that the binding/adhesion can be improved in Paunovic et al., APA and Marlin's device.

4. Claims 7, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marlin (US Pat. 6429046), Paunovic et al. (US Pat. 5294486) and APA as applied to claims 1 and 14 above, and further in view of Andricacos et al. (US Pat. 6224690) and Okamoto et al. (US Pat. 5521438).

Regarding claim 7, Marlin, Paunovic et al. and APA teach substantially the entire claimed structure as applied to claim 1 above, except the diffusion-retarding layer including a composition 54Fe-29Ni-17Co respectively.

Andricacos et al. teach the flip chip/BGA device having a variety of configurations of the UBM structure including a configuration where a layer comprising nickel or a nickel alloy such as FeNi (see Fig. 2b) is used between the binding layer and solder receiving layer for a lead-free solder to provide the adhesion and to prevent further diffusion of an intermetallic (Col. 8, lines 1-37).

Okamoto et al. teach using soldered connections comprising terminals/electrodes made of conventional Fe-Ni based alloys including commercially available Kovar and low thermal expansion Kovar, such Fe-Ni-Co alloys having different wt.%/amount of Ni, Fe and Co (Col. 6, lines 65- Col. 8, line 65) to provide the desired joining strength, reduced thermal stress and improved reliability (Col. 6-12).

Furthermore, arriving at an optimum alloy composition from effective variables such as wt.% of various components/elements in the alloy composition involves routine skill in the art of chip packaging and interconnect technology to achieve the desired final properties in the bonding material such as bonding strength, adhesion, diffusion resistance, etc [see *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (1980)].

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the diffusion retarding layer including Kovar or a composition 54Fe-29Ni-17Co as taught by Andricacos et al. and Okamoto et al. so that

the diffusion resistance and adhesion/bonding can be improved in Paunovic et al., APA and Marlin's device.

Regarding claims 15 and 17, Marlin, Paunovic et al., APA, Andricacos et al. and Okamoto et al. teach substantially the entire claimed structure as applied to claims 14, 1 and 7 above.

4. Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marlin (US Pat. 6429046), Paunovic et al. (US Pat. 5294486) and APA and as applied to claim 1, and further in view of Andricacos et al. (US Pat. 6224690) and Shimokawa et al. (US Pat. 2002/0163085).

Regarding claims 28-30, Marlin, Paunovic et al. and APA teach substantially the entire claimed structure as applied to claims 1 above, except the pad including an intermetallic compound including Ni-Sn/Ni3Sn4 and Ni-Fe.

Andricacos et al. teach the flip chip/BGA device having a variety of configurations of the UBM structure including a configuration where a layer comprising nickel or a nickel alloy such as FeNi (see Fig. 2b) is used between the binding layer and solder receiving layer for a lead-free solder containing Sn to provide the adhesion and to prevent further diffusion of an intermetallic (Col. 8, lines 1-37).

Andricacos et al. further teach intermetallics such as Ni-Sn being formed at an interface when elements such as Ni and Sn are present in the pad layers and the solder (Col. 5, lines 25-32). Shimokawa et al. teach intermetallic compound such as Sn-Fe being formed at an interface when elements such as Sn and Fe are present in the solder alloy and the solder alloy (Col. 5, lines 25-32).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the pad including the intermetallic compound including Ni-Sn/Ni3Sn4 and Ni-Fe as taught by Andricacos et al. and Shimokawa et al. so that the desired intermetallics remain adhered at the interface and further diffusion can be prevented in Paunovic et al., APA and Marlin's device.

Response to Arguments

5. Applicant's arguments filed on 09-19-05 have been fully considered but they are not persuasive.

A. Applicant argues that Paunovic et al's reference does not deal with the out-diffusion of the electrically conductive material from the pad to the solder ball and Paunovic et al. deals with controlling the movement of atoms/diffusion between layers in the pad or within the film.

However, as explained in the rejections above, Paunovic et al. disclose the prior art (see Col. 1, lines 50-65 in Paunovic et al.; the prior art: US Pat. 4016050 by Lesh et al.) where Lesh et al. teach using a conventional diffusion barrier structure wherein a

diffusion retarding layer such as nickel having a predetermine thickness is used to control/retard diffusion/out-diffusion of copper from an underlying conductor/pad layer see the prior art: Lesh et al, Col. 3, lines 23-37). Such diffusion retarding layer structure further showing satisfactory/compatible soldering having the desired electrical performance and improved soldering (see Lesh et al.: Abstract and Col. 5, line 20- Col. 6, line 16) and furthermore, such diffusion retarding layer structure is identical to the claimed structure.

B. Applicant argues (see response F: claim 7) that Examiner contends Okamoto et al. teach preventing further diffusion of the intermetallic, however there is no mention of such disclosure in Okamoto et al's reference.

However, claim 7 rejections set forth by Okamoto et al. (see page 8 of previous rejection dated 06-15-05) do not include mention of such teaching by Okamoto et al. as presented in applicant's arguments above.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the

status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

Nitin Parekh

PRIMARY EXAMINER

NP

TECHNOLOGY CENTER 2800

11-29-05